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VHDL is a strongly typed language which implies that one has always to declare the type of every object that can have a value, such as signals, constants and variables. a. Entity Declaration . The entity declaration defines the NAME of the entity and lists the input and output ports. The general form is as follows,

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VHDL is a large and verbose language with many complex constructs that have complex semantic meanings and is difficult to understand initially (VHDL is often quoted to be an acronym for Very Hard Description Language). However, it is possible to quickly understand a subset of VHDL which is both simple and easy to use.

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VHDL Primer, A, 3rd Edition. J. Bhasker (Ph.D., University of Minnesota) is a member of the Technical Staff at AT&T Bell Laboratories, Allentown, PA, where he is currently working on a high-level synthesis tool that would synthesize net-lists from C or VHDL behavioral descriptions. He teaches courses on VHDL and VHDL Synthesis to internal AT&T designers as well as at Lehigh

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Excellent index. I have about 6 years of design experience in VHDL and 18 years of embedded C development, 34 years in Engineering, so picking up Verilog went quickly. I give a lot of credit to this book for keeping clear the big and small 'pictures' of what makes up Verilog. Highly recommend it to both new and 'seasoned' (I refuse to say 'old ...

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VHDL program (code) is used to implement digital circuit inside CPLD / FPGA, or it can be used to fabricate ASIC (Application Specific Integrated Circuit) It is very useful in developing high end, sophisticated microprocessor or micro-controller like ASIP (Application Specific Instruction Processor) or PSoC (Programmable System on Chip)

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